

REMARKS

Claims 1-3, 5-13, 15-25, and 27-30 are in the application, with claims 1-3, 5-13, 15-25, and 29 having been amended, and claims 4, 14, and 26 having been cancelled. Claims 1, 15, 21, 25, and 29 are the independent claims herein. No new matter has been added. Reconsideration and further examination are respectfully requested.

Claim Rejections

Claims 1-15 and 17-30 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,367,653 ("Coyle") and claim 16 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Coyle. Reconsideration and withdrawal of the rejections are respectfully requested.

Claims 1, 15, 21, 25, and 29

Amended independent claim 1 describes a system that comprises a configurable mask, an AND gate, and a cache. The cache has one or more configurable bits that are configurable to identify one or more sets having at least one line of information storage and a tag to identify a line of information storage. Moreover, the configurable bits are ANDed to the configurable mask.

The art of record is not seen to disclose or to suggest the above-mentioned features of amended independent claim 1. In particular, the art of record is not seen to disclose or to suggest "configurable bits ANDed to a configurable mask".

Coyle describes reconfigurable associative cache memory. At column 13, lines 20 – 50 and FIG. 8A, Coyle describes a cache reconfiguration controller. The cache reconfiguration controller reconfigures the tag array by merging one or more of the least significant bits of the tag field with line bits of the main memory address resulting in a reconfigurable associative cache memory. The reconfiguration logic has three inputs: RELOAD 321, CONFIGURATION 322, and ADDR 20. ADDR 20 is ORed by an OR-gate with CONFIGURATION 322 and the output of the OR-gate is ANDed with RELOAD 321. ADDR 20 contains one or more least

significant bits of the tag field and thus, Coyle describes tag bits ORed to the CONFIGURATION input.

Accordingly, Coyle does not disclose or suggest “configurable bits ANDed to a configurable mask”. In view of the foregoing, amended independent claim 1 is believe to be in condition for allowance. Claims 2, 3, and 5-13 depend from claim 1 and are therefore also believe to be allowable for at least the foregoing reasons.

Amended independent claims 15, 21, 25, and 29 relate to a method, a node, a method and an article of manufacture respectively, in which, configurable bits are ANDed to a configurable mask. In view of the foregoing, amended independent claims 15, 21, 25, and 29 and their related independent claims are also believed to be in condition for allowance.

CONCLUSION

The outstanding Office Action presents a number of characterizations regarding the applied references, some of which are not directly addressed by this response. Applicant does not necessarily agree with the characterizations and reserve the right to further discuss those characterizations.

For at least the reasons given above, it is submitted that the entire application is in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience. Alternatively, if there remains any question regarding the present application or any of the cited references, or if the Examiner has any further suggestions for expediting allowance of the present application, the Examiner is kindly invited to contact the undersigned via telephone at (203) 972-4982.

Respectfully submitted,



March 31, 2006
Date

Richard S. Finkelstein
Registration No. 56,534
Buckley, Maschoff & Talwalkar LLC
Attorneys for Intel Corporation.
Five Elm Street
New Canaan, CT 06840
(203) 972-4982